1. An integrated voltage regulator and reverse voltage protection circuit comprising the following:

a first double-sided extended drain field effect transistor of a first carrier type and having a source terminal coupled to a first voltage source;

a second double-sided extended drain field effect transistor of the first carrier type and also having a source terminal couple to the first voltage source, and having a drain terminal coupled to a gate terminal of the first double-sided extended drain field effect transistor of the first carrier type;

a first resistor that is coupled between the first supply voltage and a body terminal of the first double-sided extended drain field effect transistor of the first carrier type and a body terminal of the second double-sided extended drain field effect transistor of the first carrier type;

a second resistor;

a third resistor coupled with the second resistor in series between a drain terminal of the first double-sided extended drain field effect transistor of the first carrier type and a second voltage source;

an extended drain field effect transistor of a second carrier type opposite the first carrier type, having a drain terminal coupled to the drain terminal of the second double-sided extended drain field effect transistor, and having a source terminal coupled to the second voltage source; and

an amplifier having an output terminal coupled to a gate terminal of the extended drain field effect transistor of the second carrier type.

WORKMAN, NYDEGGER & SEELEY
A PROFESSIONAL CORPORATION
ATTORNEYS AT LAW
1000 EAGLE GATE TOWER
60 EAST SOUTH TEMPLE
SALT LAKE CITY, UTAH 84111

2. A circuit in accordance with Claim 1, wherein the extended drain field effect transistor of the second carrier type is a single-sided extended drain field effect transistor of the second carrier type.

3. A circuit in accordance with Claim 1, wherein the extended drain field effect transistor of the second carrier type is a double-sided extended drain field effect transistor of the second carrier type.

4. A circuit in accordance with Claim 1, wherein the first carrier type is n-channel, and wherein the second carrier type is p-channel.

5. A circuit in accordance with Claim 1, wherein the first carrier type is p-channel, and wherein the second carrier type is n-channel.

6. A circuit in accordance with Claim 1, wherein the circuit further comprises a load circuit coupled between the drain terminal of the first double-sided extended drain field effect transistor and the second voltage source.

7. A circuit in accordance with Claim 6, wherein the circuit is integrated on a single chip.

8. A circuit in accordance with Claim 1, wherein a node between the second and third resistors is couple to a first input terminal of the amplifier.

WORKMAN, NYDEGGER & SEELEY
A PROFESSIONAL CORPORATION
ATTORNEYS AT LAW
1000 EAGLE GATE TOWER
60 EAST SOUTH TEMPLE
SALT LAKE CITY, UTAH 84111

9. A circuit in accordance with Claim 1, wherein a second input terminal of the amplifier is configured to be connected to a reference voltage.

10. A circuit in accordance with Claim 9, wherein the reference voltage is a first reference voltage, wherein a gate terminal of the second double-sided extended drain field effect transistor of the first carrier type is configured to be coupled to a second voltage reference.

11. A circuit in accordance with Claim 10, wherein the second voltage reference is different that the first voltage source by a factor equal to the absolute value of a threshold voltage of the second double-sided extended drain field effect transistor of the first carrier type.

12. A circuit in accordance with Claim 1, wherein the first double-sided extended drain field effect transistor of the first carrier type comprises the following:

a substrate; and

a gate terminal overlying the substrate over a channel region in the substrate, wherein the substrate further comprises the following:

a drain region of the first carrier type, wherein the drain region is laterally separated from the channel region by a first RESURF region of the first carrier type; and

a source region of the first carrier type, wherein the source region is laterally separated from the channel region by a second RESURF region of the first carrier type.

WORKMAN, NYDEGGER & SEELEY
A PROFESSIONAL CORPORATION
ATTORNEYS AT LAW
1000 EAGLE GATE TOWER
60 EAST SOUTH TEMPLE
SALT LAKE CITY, UTAH 84111

13. A circuit in accordance with Claim 12, wherein the substrate further comprises the following:

a third RESURF region of the first carrier type disposed laterally bordering the drain region on a side that is remote from the channel region; and

a fourth RESURF region of the first carrier type disposed laterally bordering the source region on a side that is remote from the channel region.

14. A circuit in accordance with Claim 1, wherein the first double-sided extended drain field effect transistor of the first carrier type is a first extended drain field effect transistor of the first carrier type, and the second double-sided extended drain field effect transistor of the first carrier type is a second extended drain field effect transistor of the first carrier type, the circuit further comprising the following:

a third extended drain field effect transistor of the first carrier type having a drain terminal coupled to the drain terminal of the extended drain field effect transistor of the second carrier type, and having a source terminal coupled to the drain terminal of the second extended drain field effect transistor of the first carrier type and to the gate terminal of the first extended drain field effect transistor of the first carrier type.

WORKMAN, NYDEGGER & SEELEY
A PROFESSIONAL CORPORATION
ATTORNEYS AT LAW
1000 EAGLE GATE TOWER
60 EAST SOUTH TEMPLE
SALT LAKE CITY, UTAH 84111

15. An integrated overvoltage and reverse voltage protection circuit comprising the following:

a first double-sided extended drain field effect transistor of a first carrier type and having a source terminal coupled to a first voltage source;

a second double-sided extended drain field effect transistor of the first carrier type and also having a source terminal couple to the first voltage source, and having a drain terminal coupled to a gate terminal of the first double-sided extended drain field effect transistor of the first carrier type;

a first resistor that is coupled between the first supply voltage and a body terminal of the first double-sided extended drain field effect transistor of the first carrier type and a body terminal of the second double-sided extended drain field effect transistor of the first carrier type;

a second resistor;

a third resistor coupled with the second resistor in series between the first voltage source and a second voltage source;

an extended drain field effect transistor of a second carrier type opposite the first carrier type, having a drain terminal coupled to the drain terminal of the second double-sided extended drain field effect transistor, and having a source terminal coupled to the second voltage source; and

a comparator having an output terminal coupled to a gate terminal of the extended drain field effect transistor of the second carrier type.

16. A circuit in accordance with Claim 15, wherein a node between the second and third resistors is couple to a first input terminal of the comparator.

WORKMAN, NYDEGGER & SEELEY
A PROFESSIONAL CORPORATION
ATTORNEYS AT LAW
1000 EAGLE GATE TOWER
60 EAST SOUTH TEMPLE
SALT LAKE CITY, UTAH 84111

17. A circuit in accordance with Claim 16, wherein a second input terminal of the comparator is configured to be connected to a reference voltage.

18. A circuit in accordance with Claim 17, wherein the reference voltage is a first reference voltage, wherein a gate terminal of the second double-sided extended drain field effect transistor of the first carrier type is configured to be coupled to a second voltage reference.

19. A circuit in accordance with Claim 18, wherein the second voltage reference is different that the first voltage source by a factor equal to the absolute value of a threshold voltage of the second double-sided extended drain field effect transistor of the first carrier type.

20. A circuit in accordance with Claim 15, wherein the first double-sided extended drain field effect transistor of the first carrier type is a first extended drain field effect transistor of the first carrier type, and the second double-sided extended drain field effect transistor of the first carrier type is a second extended drain field effect transistor of the first carrier type, the circuit further comprising the following:

a third extended drain field effect transistor of the first carrier type having a drain terminal coupled to the drain terminal of the extended drain field effect transistor of the second carrier type, and having a source terminal coupled to the drain terminal of the second extended drain field effect transistor of the first carrier type and to the gate terminal of the first extended drain field effect transistor of the first carrier type.

WORKMAN, NYDEGGER & SEELEY
A PROFESSIONAL CORPORATION
ATTORNEYS AT LAW
1000 EAGLE GATE TOWER
60 EAST SOUTH TEMPLE
SALT LAKE CITY, UTAH 84111

21. A method of using a double-sided extended drain field effect transistor that includes a substrate and a gate terminal overlying the substrate over a channel region in the substrate, wherein the substrate further comprises a drain region of the first carrier type that is laterally separated from the channel region by a first RESURF region of the first carrier type; and a source region of the first carrier type that is laterally separated from the channel region by a second RESURF region of the first carrier type, the method comprising the following:

an act of applying a first reverse bias to a first interface between the source region of the first carrier type and a body region of a second carrier type; and

an act of applying a second reverse bias to a second interface between the drain region of the first carrier type and the body region of the second carrier type.

22. A method in accordance with Claim 21, wherein the first reverse bias is not sufficient to breakdown the first interface, but would be sufficient to cause breakdown of the first interface if the first RESURF region and any other RESURF region bordering the source region were not present.

WORKMAN, NYDEGGER & SEELEY
A PROFESSIONAL CORPORATION
ATTORNEYS AT LAW
1000 EAGLE GATE TOWER
60 EAST SOUTH TEMPLE
SALT LAKE CITY, UTAH 84111

23. A method in accordance with Claim 22, wherein the second reverse bias is not sufficient to breakdown the second interface, but would be sufficient to cause breakdown of the second interface if the second RESURF region and any other RESURF region bordering the drain region were not present.

24. A method in accordance with Claim 21, wherein the second reverse bias is not sufficient to breakdown the second interface, but would be sufficient to cause

breakdown of the second interface if the second RESURF region and any other RESURF region bordering the drain region were not present.

WORKMAN, NYDEGGER & SEELEY
A PROFESSIONAL CORPORATION
ATTORNEYS AT LAW
1000 EAGLE GATE TOWER
60 EAST SOUTH TEMPLE
SALT LAKE CITY, UTAH 84111